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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/523,585

09/08/2005

Kenji Fukuda

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7590

03/20/2007

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EXAMINER

MATTHEWS, COLLEEN ANN

ART UNIT

PAPER NUMBER

2811

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
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3 MONTHS

03/20/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/20/2007.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/523,585	<b>Applicant(s)</b> FUKUDA ET AL.	
	<b>Examiner</b> Colleen A. Matthews	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 2-5, 11 and 17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 6-10, 12-16 and 18-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Objections*

The amendment filed 12/19/2006 could have been held non-complaint under 37 CFR 1.121, Amendments to the claims filed on or after July 30, 2003 must comply with 37 CFR 1.121(c)(2) which states: *"If a withdrawn claim is currently amended, its status in the claim listing may be identified as "withdrawn— currently amended." "* See MPEP 714.

Claims 11 and 17 are "withdrawn – currently amended" but not properly indicated as so. For sake of expediting prosecution, the claim will be examined, however a corrected section is required. Applicant is also request to review all claims to ensure that all claims that have been amended with proper indications.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1, 7 and 8 rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 6,956,238 to Ryu et al. (Ryu) in view of U.S. Pat. No. 6,664,143 to Zhang.
3. **Regarding claim 1**, Ryu discloses a MISFET comprising: an n-type silicon carbide substrate (10) of a high impurity concentration; an n-type silicon carbide layer (12) of a low impurity concentration disposed on the substrate; a first n-type silicon

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carbide region (27) of a first impurity concentration disposed on a surface of the n-type silicon carbide layer of low impurity concentration; a first p-type silicon carbide region (22/20) disposed as adjoined to opposite sides of the first n-type silicon carbide region; a second n-type silicon carbide region (24) of a second impurity concentration disposed selectively from a surface through an interior of the first p-type silicon carbide region at a position separated from the first n-type silicon carbide region; a wiring of metal (30) or polycrystalline silicon serving to short-circuit the first p-type silicon carbide region (22/20) to the second n-type silicon carbide region (24); a gate electrode (32) disposed in a surface part of each of the the p-type silicon carbide regions through a gate insulating film (28); and a third n-type silicon carbide region (26') of a third impurity concentration formed both between the first n-type silicon carbide region (27) and the first p-type silicon carbide region (22/20) below the gate electrode (32) and between the second n-type silicon carbide region (24) and the first p-type silicon carbide region below the gate electrode (22/20), selectively from the surface through the interior of the first p-type silicon carbide region (22/20); all components being individually formed in a vertical DMOS structure.

Ryu fails to disclose having a metal or an implanted impurity in the wiring (30). Zhang discloses a MISFET where a wiring is made of polycrystalline silicon having a implanted impurity (col 8 line 64 – col 9 line 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ryu to have the wiring of metal or polycrystalline silicon having a metal or an implanted impurity as in Zhang in order to have improved contact characteristics.

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4. **Regarding claims 7 and 8**, Ryu as modified discloses the device of claim 1. Ryu also discloses the gate electrode formed of a p-type polycrystalline silicon (col 15 lines 17-18). Ryu fails to disclose forming the electrode having boron implanted to a concentration of  $1 \times 10^{16}$  to  $1 \times 10^{21} \text{ cm}^{-3}$  or of n-type polycrystalline silicon having phosphorus or arsenic implanted to a concentration of  $1 \times 10^{16}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . Zhang teaches forming the electrode of p-type polycrystalline silicon having boron implanted or of n-type polycrystalline silicon having phosphorus or arsenic implanted (col 8 line 64 – col 9 line 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ryu to have the electrode p-type polycrystalline silicon having boron implanted or of n-type polycrystalline silicon having phosphorus or arsenic implanted as in Zhang in order to have improved contact characteristics.

Ryu as modified by Zhang fails to disclose the implanted impurities to a concentration of  $1 \times 10^{16}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . However, one of ordinary skill in the art must balance many known factors when designing and optimizing a device. As such, varying the concentration would not be cause for undue experimentation. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) see MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the concentration of  $1 \times 10^{16}$  to  $1 \times 10^{21} \text{ cm}^{-3}$  in order to improve contact characteristics

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5. **Claims 6 and 9 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 6,956,238 to Ryu et al. (Ryu) in view of U.S. Pat. No. 6,664,143 to Zhang in further view of U.S. Pub. No. 2001/0025994 to Yoshino et al. (Yoshino).

6. **Regarding claims 6 and 9**, Ryu as modified above discloses the device of claim 1. Ryu fails to disclose the gate electrode formed of aluminum, aluminum containing alloy or molybdenum. Ryu also fails to disclose a silicide film deposited on the gate electrode, where the silicide film is formed of silicon and any one of tungsten, molybdenum and titanium.

Yoshino teaches a gate electrode formed of aluminum (paragraph 0036 line 4) and Yoshino also teaches a tungsten silicide film on the gate electrode (paragraph 0036 lines 6-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ryu to have the gate electrode formed of aluminum and a tungsten silicide film on the gate electrode as in Yoshino in order to achieve desired electrical resistivity.

7. **Claims 10, 13-14, 16 and 19-20 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 6,956,238 to Ryu et al. (Ryu) in view of U.S. Pat. No. 6,664,143 to Zhang in further view of U.S. Pub. No. 2001/0038108 to Kitabatake et al. (Kitabatake).

8. **Regarding claims 10, 13-14, 16 and 19-20**, Ryu as modified discloses the device of claims 1, 7 and 8 as above, including the n-type silicon carbide layer of low

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impurity concentration (12) formed on a face of the n-type substrate of a high impurity concentration (10).

Ryu as modified fails to disclose using a (11-20) or (000-1) face of the substrate or the substrate made of tetragonal or rhombohedral silicon carbide single crystal. Kitabatake teaches a substrate made of rhombohedral silicon carbide single crystal (paragraph [0041] line 6, 15R-SiC). Kitabatake also disclose using the (11-20) and (000-1) face of the substrate for (paragraph [0009] line 5 and paragraph [0041] line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ryu to have the substrate made of rhombohedral silicon carbide single crystal and to use to use a (11-20) or (000-1) face of the substrate as in Kitabatake in order to more easily grow the low impurity concentration layer on the substrate and to adjust manufacturing properties such as oxidation rate.

9. **Claims 12, 15, 18 and 21 are rejected under 35 U.S.C. 103(a)** as being unpatentable over U.S. Pat. No. 6,956,238 to Ryu et al. (Ryu) in view of U.S. Pat. No. 6,664,143 to Zhang in view of U.S. Pub. No. 2001/0025994 to Yoshino et al. (Yoshino) in further view of U.S. Pub. No. 2001/0038108 to Kitabatake et al. (Kitabatake).

10. **Regarding claims 12, 15, 18 and 21**, Ryu as modified discloses the device of claims 6 and 9 as above, including the n-type silicon carbide layer of low impurity concentration (12) formed on a face of the n-type substrate of a high impurity concentration (10).

Ryu as modified fails to disclose using a a (11-20) or (000-1) face of the substrate or the substrate made of tetragonal or rhombohedral silicon carbide single crystal. Kitabatake teaches a substrate made of rhombohedral silicon carbide single crystal (paragraph [0041] line 6, 15R-SiC). Kitabatake also disclose using the (11-20) and (000-1) face of the substrate for (paragraph [0009] line 5 and paragraph [0041] line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ryu to have the substrate made of rhombohedral silicon carbide single crystal and to use to use a (11-20) or (000-1) face of the substrate as in Kitabatake in order to more easily grow the low impurity concentration layer on the substrate and to adjust manufacturing properties such as oxidation rate.

### ***Response to Arguments***

Applicant's arguments filed 12/19/2006 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., two gate electrodes separated sideward, Remarks page 10 paragraph 1) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).



Applicant argues (Remarks, page 10, paragraph 2) that Ryu's wiring (30) is not configured to short circuit first p-type silicon carbide regions (20) to second n-type silicon carbide regions (24). However, as clarified above, first p-type silicon carbide region can be considered both areas 20 and 22. And as Figure 7 of Ryu clearly shows wiring (30) in contact with both region (22/20) and (24)

In response to applicant's arguments against the references individually (Remarks pages 11-12), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

### **Conclusion**

Applicant's amendment to claims 10, 12-16, and 18-21 necessitated the new ground(s) of rejection presented for these claims in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAM  
03/14/2007

  
Sara Crane  
Primary Examiner